GE866-QUAD Hardware User Guide

1VV0301051 Rev. 3 – 2014-09-10

Making machines talk.

APPLICABILITY TABLE

PRODUCT
GE866-QUAD

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1. Introduction

1.1. Scope

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit GE866-QUAD module.

1.2. Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our GE866-QUAD modules.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

To register for product news and announcements or for product questions contact Telit Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

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1.4. Document Organization

This document contains the following chapters:

Chapter 1: "Introduction" provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: "Overview" provides an overview of the document.

Chapter 3: "GE866-QUAD Mechanical Dimensions"

Chapter 4: "GE866-QUAD Module Connections" deals with the pin out configuration and layout.

Chapter 5: "Hardware Commands" How to operate on the module via hardware.

Chapter 6: "Power supply" Power supply requirements and general design rules.

Chapter 7: "Antenna" The antenna connection and board layout design are the most important parts in the full product design.

Chapter 8: "Logic Level specifications" Specific values adopted in the implementation of logic levels for this module.

Chapter 9: "Serial ports" The serial port on the Telit GE866-QUAD is the core of the interface between the module and OEM hardware

Chapter 10: "Audio Section overview" Refers to the audio blocks of the Base Band Chip of the GE866-QUAD Telit Modules.

Chapter 11: "General Purpose I/O" How the general purpose I/O pads can be configured.

Chapter 12 "DAC and ADC Section" Deals with these two kind of converters.

Chapter 13: "Mounting the GE866 on your Board" Recommendations and specifics on how to mount the module on the user's board.

Chapter 14: "Packing system" Recommendations and specifics on how the system is packaged.

Chapter 15: "Safety Recommendations" Recommendations and specifics on how the system is packaged.

Chapter 16: "Document History" Holds all document changes

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1.5. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.6. Related Documents

- Telit GSM/GPRS Family Software User Guide, 1vv0300784
- Audio settings application note , 80000NT10007a
- Digital Voice Interface Application Note, 80000NT10004a
- GE866-QUAD Product description, 80416ST10122A
- SIM Holder Design Guides, 80000NT10001a
- AT Commands Reference Guide, 80000ST10025a
- Telit EVK2 User Guide, 1vv0300704

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2. Overview

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit GE866-QUAD module.

In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace all hardware solutions and products that may be designed. Avoiding the wrong solutions shall be considered as mandatory. While the suggested hardware configurations shall not be considered mandatory, the information given shall be used as a guide and a starting point for properly developing your product with the Telit GE866-QUAD module.

NOTE:

The integration of the GSM/GPRS GE866-QUAD cellular module within user application shall be done according to the design rules described in this manual.

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3. GE866-QUAD Mechanical Dimensions

The GE866-QUAD overall dimensions are:

- Length: 19 mm
- Width: 15 mm
- Thickness: 2.2 mm

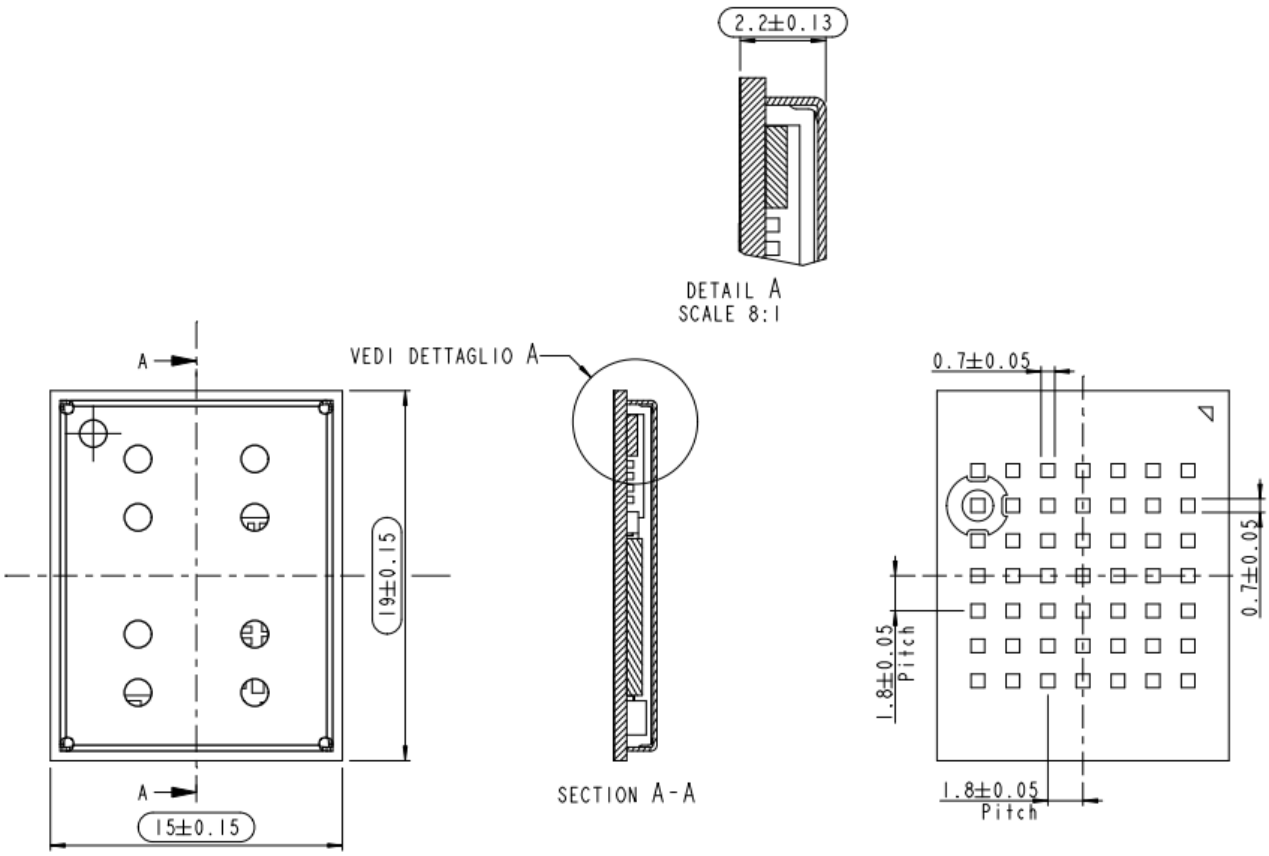

Figure 1

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4. GE866-QUAD module connections

4.1. PIN-OUT

Pad	Signal	I/O	Function	Note	Type
Audio					
E7	EAR-	AO	Earphone signal output, phase -		Audio
D7	EAR+	AO	Earphone signal output, phase +		Audio
G7	MIC-	AI	Mic. signal input; phase-		Audio
F7	MIC+	AI	Mic. signal input; phase+		Audio
F6	AGND	-	Analog Ground		Power
SIM card interface					
C7	SIMVCC	-	External SIM signal – Power supply for the SIM		1,8 / 3V
B7	SIMRST	O	External SIM signal – Reset		1,8 / 3V
A7	SIMCLK	O	External SIM signal – Clock		1,8 / 3V
A6	SIMIO	I/O	External SIM signal – Data I/O	4.7k Pull up	1,8 / 3V
X All GPI0 can be program med	SIMIN	I	Presence SIM input		CMOS 1.8V
Trace					
C2	RXD_AUX	I	Auxiliary UART (RX Data)		CMOS 1.8V
C1	TXD_AUX	O	Auxiliary UART (TX Data)		CMOS 1.8V
Prog. / Data + HW Flow Control					
B2	C109/DCD/GPO	O	Output for Data carrier detect signal (DCD) to DTE / GP output		CMOS 1.8V
B3	C125/RING/GPO	O	Output for Ring indicator signal (RI) to DTE / GP output		CMOS 1.8V
A3	C107/DSR/GPO	O	Output for Data set ready signal (DSR) to DTE / GP output		CMOS 1.8V
A2	C108/DTR/GPI	I	Input for Data terminal ready signal (DTR) from DTE / GP input		CMOS 1.8V
A1	C105/RTS/GPI	I	Input for Request to send signal (RTS) from DTE / GP input		CMOS 1.8V
B1	C106/CTS/GPO	O	Output for Clear to send signal (CTS) to DTE / GP output		CMOS 1.8V
A4	C103/TXD	I	Serial data input (TXD) from DTE		CMOS 1.8V
A5	C104/RXD	O	Serial data output to DTE		CMOS 1.8V
DAC and ADC					
F4	ADC_IN	AI	Analog/Digital converter input		A/D
E4	DAC_OUT	AO	Digital/Analog converter output		D/A
Miscellaneous Functions					
F5	VRTC	AO	VRTC Backup	2.3V	Power

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Pad	Signal	I/O	Function	Note	Type
G4	RESET*	I	Reset input		CMOS 1.8V
G6	V_AUX / PWRMON	O	1.8V stabilized output Imax=100mA / Power ON monitor		Power Out 1.8V
G2	Antenna	I/O	Antenna pad – 50 Ω		RF
GPIO					
C5	GPIO_01 / DVI_WA0	I/O	GPIO01 Configurable GPIO / Digital Audio Interface (WA0)		CMOS 1.8V
C6	GPIO_02 / JDR / DVI_RX	I/O	GPIO02 I/O pin / Jammer Detect Report / Digital Audio Interface (RX)		CMOS 1.8V
D6	GPIO_03 / DVI_TX	I/O	GPIO03 GPIO I/O pin / Digital Audio Interface (TX)		CMOS 1.8V
D5	GPIO_04 / TX Disable / DVI_CLK	I/O	GPIO04 Configurable GPIO / TX Disable input / Digital Audio Interface (CLK)		CMOS 1.8V
B5	GPIO_05 / RFTXMON	I/O	GPIO05 Configurable GPIO / Transmitter ON monitor		CMOS 1.8V
B4	GPIO_06 / ALARM / BUZZER	I/O	GPIO06 Configurable GPIO / ALARM		CMOS 1.8V
C4	GPIO_07 / STAT_LED	I/O	GPIO07 Configurable GPIO / Digital Audio Interface (CLK)		CMOS 1.8V
Power Supply					
E2	VBATT	-	Main power supply (Baseband)		Power
E1	VBATT_PA	-	Main power supply (Radio PA)		Power
F6	AGND	-	AF Signal Ground (see audio section)		AF Signal
D1	GND	-	Ground		Power
F1	GND	-	Ground		Power
G1	GND	-	Ground		Power
D2	GND	-	Ground		Power
F2	GND	-	Ground		Power
C3	GND	-	Ground		Power
E3	GND	-	Ground		Power
F3	GND	-	Ground		Power
G3	GND	-	Ground		Power
RESERVED					
D3		-			
D4		-			
E5		-			
G5		-			
B6		-			
E6		-			

WARNING:

Reserved pins must not be connected.

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WARNING:

VAUX output must not be used to supply any device on the customer application.

It is only provided as reference/supply voltage when voltage translation to 1V8 CMOS is needed.

When its use is necessary, it is strongly recommended to connect VAUX through a series resistor as closed as possible to the module in order to reduce the inrush current of the internal DC/DC supply. Use a low value resistor (e.g. 10 ohm, 1/3W) with a maximum power rating related to drained current.

NOTE:

If not used, almost all pins should be left disconnected. The only exceptions are the following pins:

Pin	signal
E2, E1	VBATT & VBATT_PA
D1, F1, G1, D2, F2, C2, E3, F3, G3	GND
F6	AGND
A4	TXD
A5	RXD
A1	RTS
G6	V_AUX / PWRMON
G4	RESET*
C1	TXD_AUX
C2	RXD_AUX

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4.2. Pin Layout

TOP VIEW

	A	B	C	D	E	F	G
1	C105/RTS	C106/CTS	TXD_AUX	GND	VABTT_PA	GND	GND
2	C108/DTR	C109/DCD	RXD_AUX	GND	VABTT	GND	ANT
3	C107/DSR	C125/RING	GND	RESERVED	GND	GND	GND
4	C103/TXD	GPIO_06/ ALRM/ BUZZER	GPIO_07/ STAT_LED	RESERVED	DAC_OUT	ADC_IN	RESET*
5	C104/RXD	GPIO_05/ RFTXMON	GPIO_01/ DVI_WAO	GPIO_04/ TX_DIS/ DVI_CLK	RESERVED	VRTC	RESERVED
6	SIMIO	RESERVED	GPIO_02/ JDR/ DVI_RX	GPIO_03/ DVI_TX	RESERVED	AGND	V_AUX/ PWRMON
7	SIMCLK	SIMRST	SIMVCC	EAR+	EAR-	MIC+	MIC-

AUDIO
SIM
MISCELLANOUS
SERIAL
GPIO

ANTENNA
RESERVED/FU
POWER
GND

NOTE:

The pins defined RESERVED must not be connected to any pin in the application.

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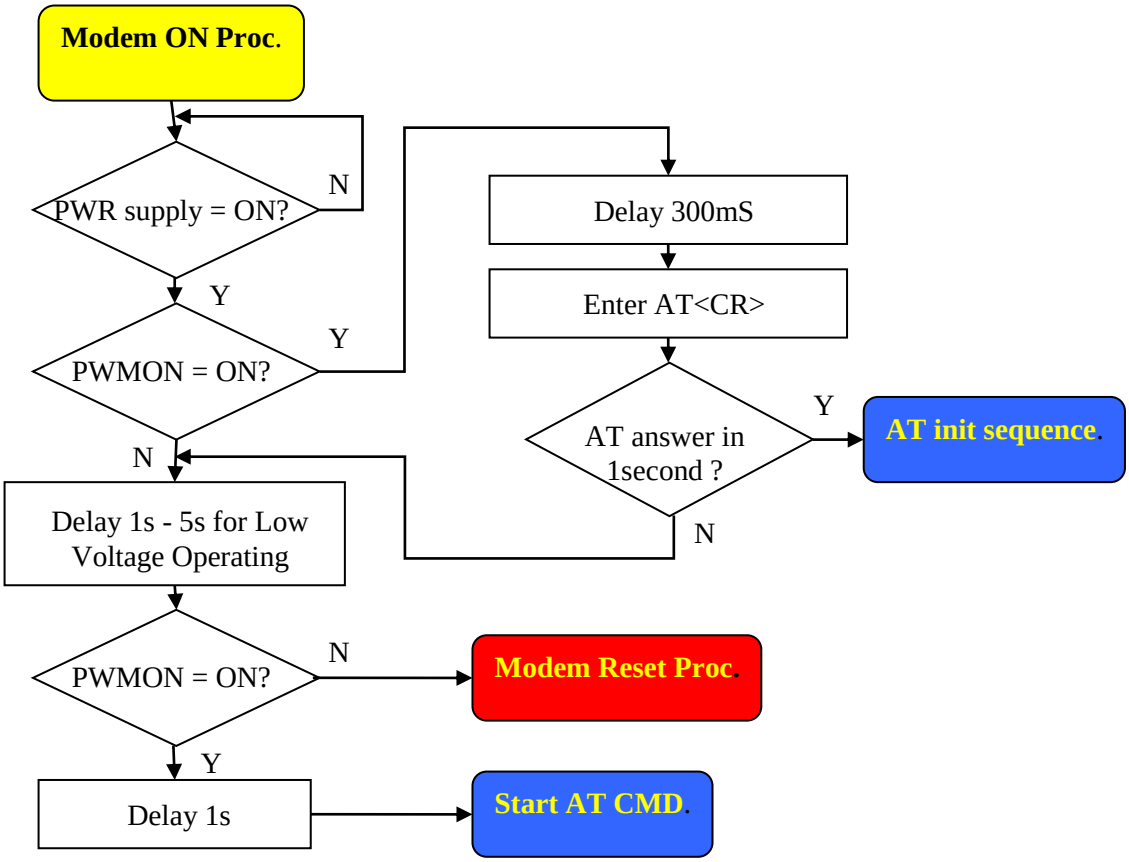
5. Hardware Commands

5.1. Auto-Turning ON the GE866-QUAD

To Auto-turn on the GE866-QUAD, the power supply must be applied on the power pins VBATT and VBATT_PA, after 1000 m-seconds, the V_AUX / PWRMON pin will be at the high logic level and the module can be considered fully operating.

When the power supply voltage is between 3.22V and 3.4V, after 5000 m-seconds, the V_AUX / PWRMON pin will be at the high logic level and the module can be considered fully operating.

The following flow chart shows the proper turn on procedure:



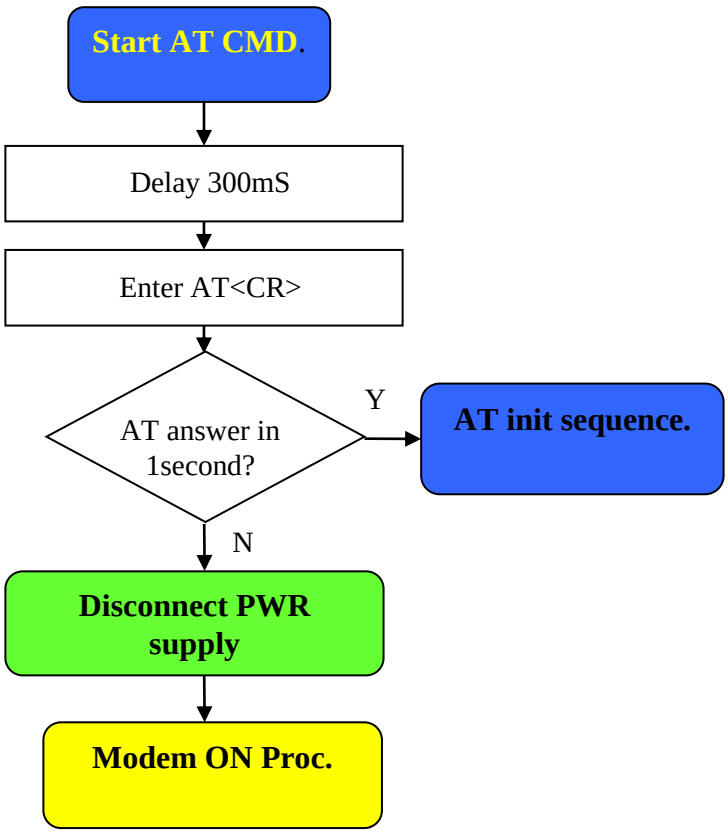
NOTE:

The power supply must be applied either at the same time on pins VBATT and VBATT_PA, or first applied on VBATT_PA and then on VBATT. The opposite sequence shall be avoided. The reverse procedure applies for powering down the module: first disconnect VBATT, then VBATT_PA, or both at once.

NOTE:

In order to prevent a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the GE866-QUAD when the module is powered OFF or during an ON/OFF transition.

A flow chart showing the AT commands managing procedure is displayed below:



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5.2. Turning OFF the GE866-QUAD

Turning off of the device can be done in two ways:

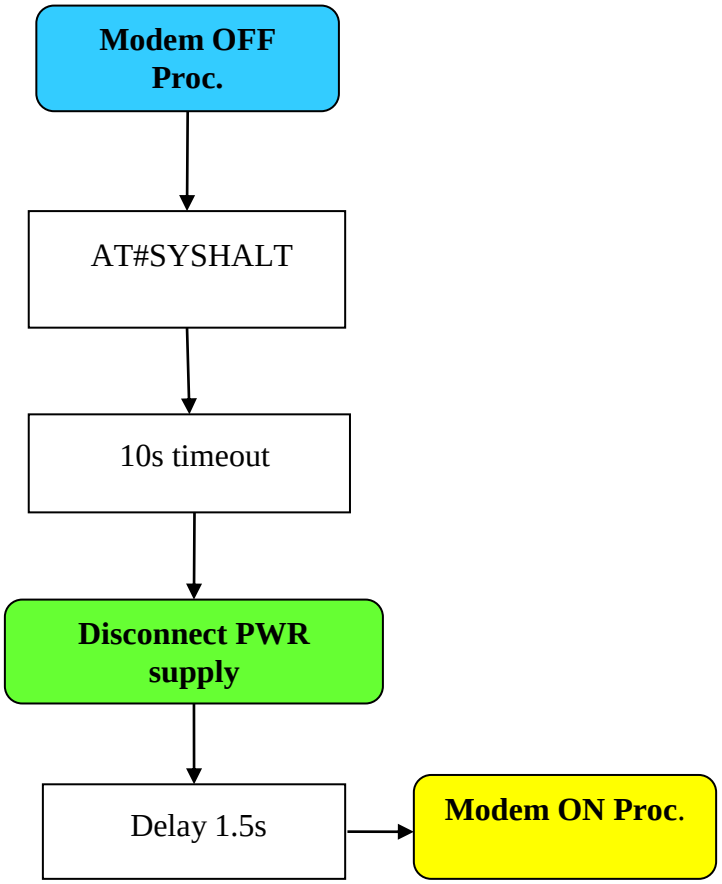
- General turn OFF
- Processor turn OFF

General turn OFF – disconnect the power supply from the both power pins VBATT and VBATT_PA at the same time. In this case all parts of the module are in OFF condition, no power consumption is present.

Processor turn OFF – disconnect the power supply only from the power pin VBATT, the power pin VBATT_PA can be connected to power supply, in this case a low, about 30uA, power consumption is present

Before either of both OFF procedures is applied, the AT#SYSHALT AT command must be sent (see AT Commands Reference Guide, 80000ST10025a), after the OK response message, wait for 10 seconds, then the module can be consider fully not operating and at this moment is possible disconnect the Power Supply.

The following flow chart shows the proper turnoff procedure:



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WARNING:

PWRMON can be used to monitor only the power on but it cannot be used to monitor the power off because it remains high

NOTE:

In order to prevent a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the GE866-QUAD when the module is powered off or during an ON/OFF transition.

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5.3. Resetting the GE866-QUAD

5.3.1. Hardware Unconditional restart

WARNING:

The hardware unconditional Restart must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure to be done in the rare case that the device gets stuck waiting for some network or SIM responses.

To unconditionally reboot the GE866-QUAD, the pad RESET* must be tied low for at least 200 milliseconds and then released.

The maximum current that can be drained from the ON* pad is 0.15 mA.

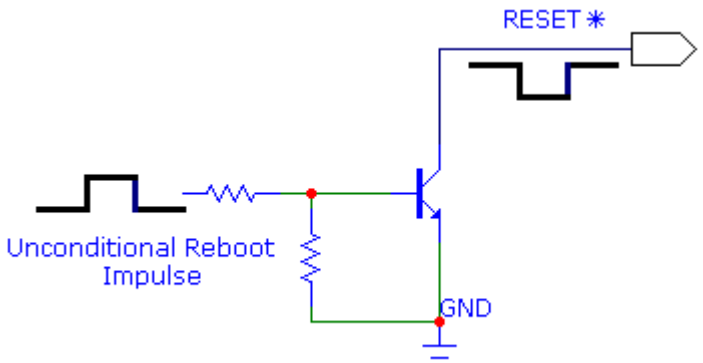
NOTE:

Do not use any pull up resistor on the RESET* line nor any totem pole digital output. Using pull up resistor may bring to latch up problems on the GE866-QUAD power regulator and improper functioning of the module. The line RESET* must be connected only in open collector configuration; the transistor must be connected as close as possible to the RESET* pin.

TIP:

The unconditional hardware restart must always be implemented on the boards and the software must use it as an emergency exit procedure.

A simple circuit to do it is:



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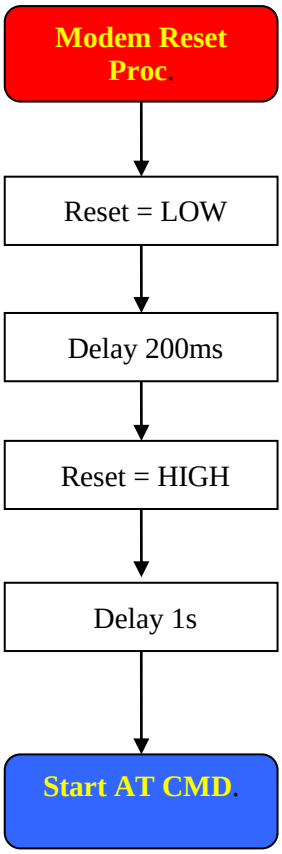
In the following flow chart is detailed the proper restart procedure:



NOTE:

In order to prevent a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the GE866-QUAD when the module is powered OFF or during an ON/OFF transition.

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6. Power Supply

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performance, hence read the requirements carefully and the guidelines that will follow for a proper design.

6.1. Power Supply Requirements

The external power supply must be connected to VBATT & VBATT_PA signals and must fulfill the following requirements:

POWER SUPPLY	
Nominal Supply Voltage	3.8 V
Normal Operating Voltage Range	3.40 V÷ 4.20 V
Extended Operating Voltage Range	3.10 V÷ 4.50 V

NOTE:

The Operating Voltage Range MUST never be exceeded; care must be taken when designing the application's power supply section to avoid having an excessive voltage drop.

If the voltage drop is exceeding the limits it could cause a Power Off of the module.

The Power supply must be higher than 3.22 V to power on the module.

NOTE:

Overshoot voltage (regarding MAX Extended Operating Voltage) and drop in voltage (regarding MIN Extended Operating Voltage) MUST never be exceeded;

The "Extended Operating Voltage Range" can be used only with complete assumption and application of the HW User guide suggestions.

NOTE:

When the power supply voltage is between 3.22V and 3.4V, after 5000 m-seconds, the V_AUX / PWRMON pin will be at the high logic level and the module can be consider fully operating. See Par. 5.1.

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6.2. Power Consumption

The GE866-QUAD preliminary power consumptions are:

GE866-QUAD		
Mode	**Average (mA)**	**Mode description**
SWITCHED OFF		Module power supplied only on VBATT_PA pin, the VBATT pin is not power supplied.
Switched Off	Typical 2uA max 20uA	
Switched Off with AT#SYSHALT	<500uA	Module power supplied on VBATT_PA pin and VBATT pin, the command AT#SYSHALT is applied.
IDLE mode		
AT+CFUN=1	9	Normal mode: full functionality of the module
AT+CFUN=4	9	Disabled TX and RX; module is not registered on the network
AT+CFUN=0 or =5	1.7	Paging Multiframe 2
	1.5	Paging Multiframe 3
	1.3	Paging Multiframe 4
	0,9	Paging Multiframe 9
CSD TX and RX mode		GSM VOICE CALL
GSM900 CSD PL5	200	
DCS1800 CSD PL0	150	
GPRS (class 1) 1TX + 1RX		GPRS Sending data mode
GSM900 PL5	200	
DCS1800 PL0	140	
GPRS (class 10) 2TX + 3RX		GPRS Sending data mode
GSM900 PL5	330	
DCS1800 PL0	250	

The GSM system is made in a way that the RF transmission is not continuous, but it is packed into bursts at a base frequency of approx. 217 Hz, and the relative current peaks can be as high as about 2A. Therefore the power supply has to be designed to withstand these current peaks without big voltage drops; this means that both the electrical design and the board layout must be designed for this current flow.

If the layout of the PCB is not well designed a strong noise floor is generated on the ground and the supply; this will reflect on all the audio paths producing an audible annoying noise at approx. 217 Hz; if the voltage drop during the peak current absorption is too much, then the device may even shutdown as a consequence of the supply voltage drop.

NOTE:

The electrical design for the Power supply should be made ensuring it will be capable of a peak current output of at least 2 A.

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6.3. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- The electrical design
- The thermal design
- Thermal PCB layout

6.3.1. Electrical Design Guidelines

The electrical design of the power supply depends strongly on the power source from which this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

6.3.1.1. + 5V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suited because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the GE866-QUAD, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the GE866-QUAD from power polarity inversion.

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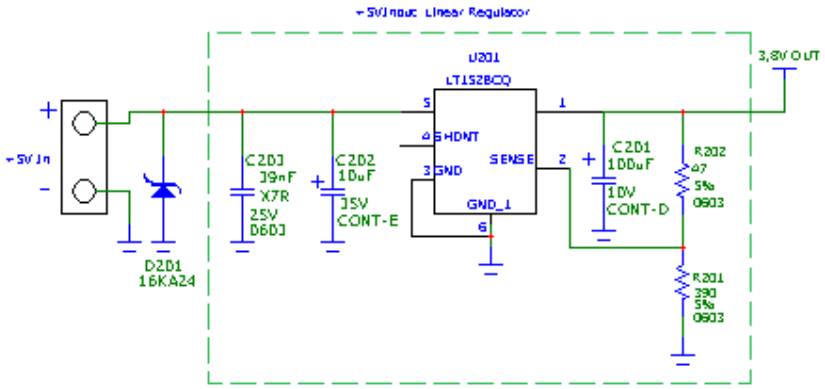
An example of linear regulator with 5V input is:



6.3.1.2. + 12V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency especially with the 2A peak current load represented by the GE866-QUAD.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15,8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For Car applications a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.
- A protection diode should be inserted close to the power input, in order to save the GE866-QUAD from power polarity inversion. This can be the same diode as for spike protection.

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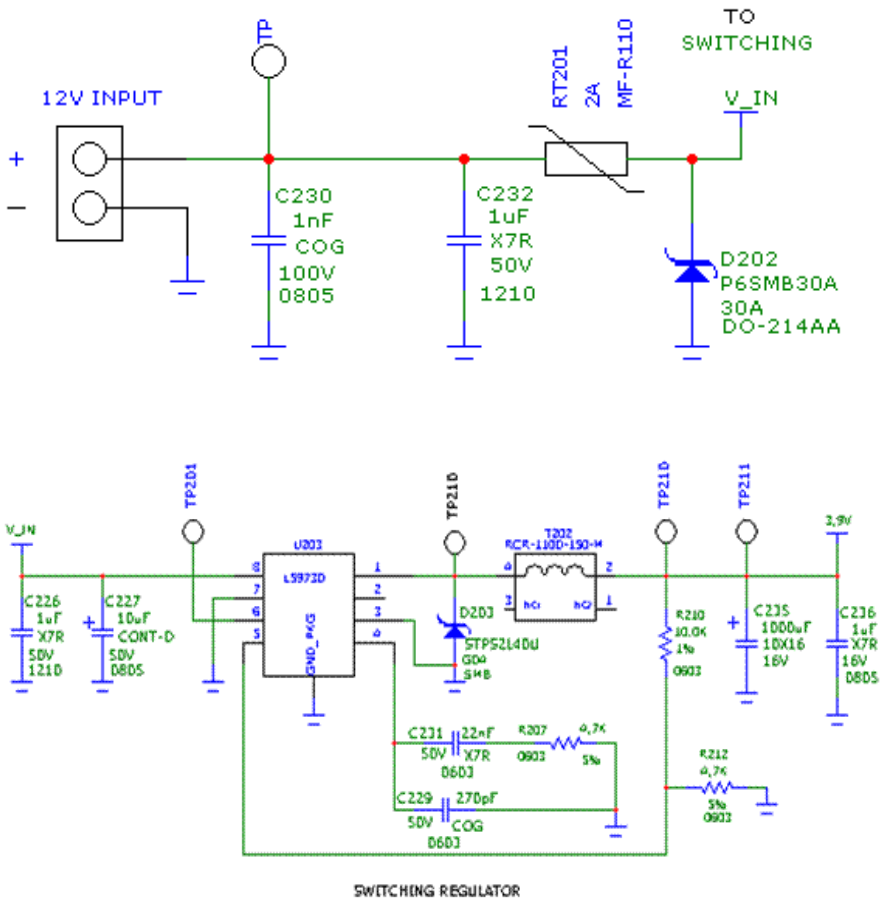
An example of switching regulator with 12V input is in the below schematic:



6.3.1.3. Battery Source Power Supply Design Guidelines

- The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V, hence a single 3.7V Li-Ion cell battery type is suited for supplying the power to the Telit GE866-QUAD module.

WARNING:

The three cells Ni/Cd or Ni/MH 3.6 V Nom. battery types or 4V PB types MUST NOT BE USED DIRECTLY since their maximum voltage can rise over the absolute maximum voltage for the GE866-QUAD and damage it.

NOTE:

DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with GE866-QUAD. Their use can lead to overvoltage on the GE866-QUAD and damage it. USE ONLY Li-Ion battery types.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the GE866-QUAD from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The battery capacity must be at least 500mAh in order to withstand the current peaks of 2A; the suggested capacity is from 500mAh to 1000mAh.

6.3.2. Thermal Design Guidelines

The thermal design for the power supply heat sink should be done with the following specifications:

See Par. 6.2 Power Consumption

NOTE:

The average consumption during transmissions depends on the power level at which the device is requested to transmit by the network. The average current consumption hence varies significantly.

Considering the very low current during idle, especially if Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.

For the heat generated by the GE866-QUAD, you can consider it to be during transmission 1W max during CSD/VOICE calls and 2W max during class10 GPRS upload.

This generated heat will be mostly conducted to the ground plane under the GE866-QUAD; you must ensure that your application can dissipate it.

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6.3.3. Power Supply PCB layout Guidelines

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performance.

- The Bypass low ESR capacitor must be placed close to the Telit GE866-QUAD power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the GE866-QUAD is wide enough to ensure a dropless connection even during the 2A current peaks.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when the 2A current peaks are absorbed. Note that this is not made in order to save power loss but especially to avoid the voltage drops on the power line at the current peaks frequency of approx. 217 Hz that will reflect on all the components connected to that supply, introducing the noise floor at the burst base frequency. For this reason while a voltage drop of 300-400 mV may be acceptable from the power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If your application doesn't have audio interface but only uses the data feature of the Telit GE866-QUAD, then this noise is not so disturbing and power supply layout design can be more forgiving.
- The PCB traces to the GE866-QUAD and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 2A current peaks are absorbed. This is for the same reason as previous point. Try to keep this trace as short as possible.
- The PCB traces connecting the Switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- The use of a good common ground plane is suggested.
- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.

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7. Antenna

The antenna connection and board layout design are the most important aspect in the full product design as they strongly affect the product overall performance, hence read carefully and follow the requirements and the guidelines for a proper design.

7.1. GSM Antenna Requirements

As suggested on the Product Description the antenna and antenna transmission line on PCB for a Telit GE866-QUAD device shall fulfill the following requirements:

ANTENNA REQUIREMENTS	
Frequency range	824-894 MHz GSM850 band 880-960 MHz GSM900 band 1710-1885MHz DCS1800 band 1850-1990MHz PCS1900 band
Gain	1.4dBi @ GSM900 and 3dBi @ DCS1800 1.4dBi @ GSM850 and 3dBi @ PCS1900
Impedance	50 Ohm
Input power	> 2 W
VSWR absolute max	≤ 10:1 (limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (limit to fulfill all regulatory requirements)

7.1.1. GE866-QUAD Antenna – PCB line Guidelines

When using the Telit GE866-QUAD module, since there's no antenna connector on the module, the antenna must be connected to the GE866-QUAD through the PCB with the antenna pad (**pin G2**).

WARNING:

High Frequency harmonics may still not be sufficiently attenuated in the GE866's small package. The suggested Pi network, between antenna output of the module and antenna connector on application board, is used to meet the standard specifications.

In first designs its use is strongly recommended.

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In the case that the antenna is not directly developed on the same PCB, hence directly connected at the antenna pad of the GE866-QUAD, then a PCB line is needed in order to connect with it or with its connector.

This transmission line shall fulfill the following requirements:

ANTENNA LINE ON PCB REQUIREMENTS	
Impedance	50 ohm
Max Attenuation	0,3 dB
No coupling with other signals allowed	
Cold End (Ground Plane) of antenna shall be equipotential to the GE866-QUAD ground pins	

This transmission line should be designed according to the following guidelines:

- Ensure that the antenna line impedance is 50 ohm;
- Keep the antenna line on the PCB as short as possible, since the antenna line loss shall be less than 0,3 dB;
- Antenna line must have uniform characteristics, constant cross section, avoid meanders and abrupt curves;
- Keep, if possible, one layer of the PCB used only for the Ground plane;
- Surround (on the sides, over and under) the antenna line on PCB with Ground, avoid having other signal tracks facing directly the antenna line track;
- The ground around the antenna line on PCB has to be strictly connected to the Ground Plane by placing vias every 2mm at least;
- Place EM noisy devices as far as possible from GE866-QUAD antenna line;
- Keep the antenna line far away from the GE866-QUAD power supply lines;
- If you have EM noisy devices around the PCB hosting the GE866-QUAD, such as fast switching ICs, take care of the shielding of the antenna line by burying it inside the layers of PCB and surround it with Ground planes, or shield it with a metal frame cover.
- If you don't have EM noisy devices around the PCB of GE866-QUAD, by using a micro strip on the superficial copper layer for the antenna line, the line attenuation will be lower than a buried one.

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7.2. PCB Design Guidelines

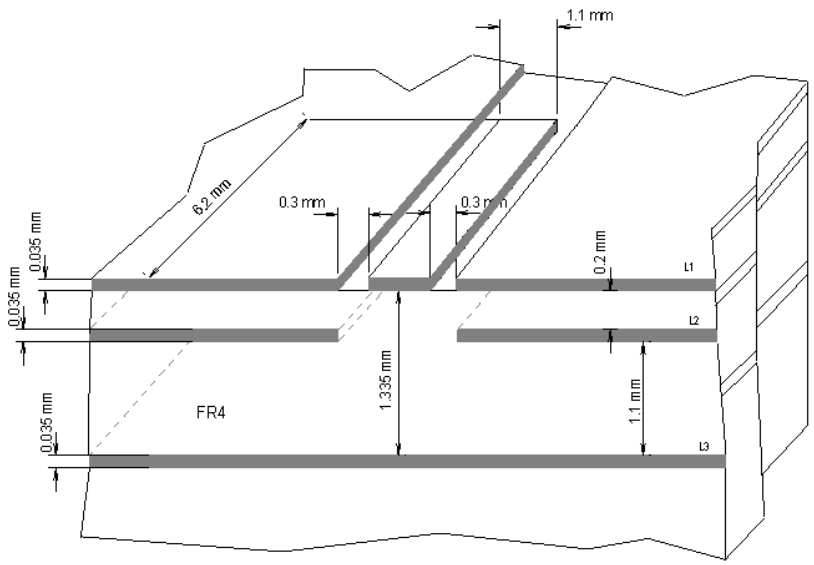
This section explains the suggested design for the transmission line on the customer's application board.

7.2.1. Transmission line design

During the design of the GE866-QUAD interface board, the placement of components has been chosen properly, in order to keep the line length as short as possible, thus leading to lowest power losses possible. A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line.

The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity εr = 4.6 ± 0.4 @ 1 GHz, TanD= 0.019 ÷ 0.026 @ 1 GHz.

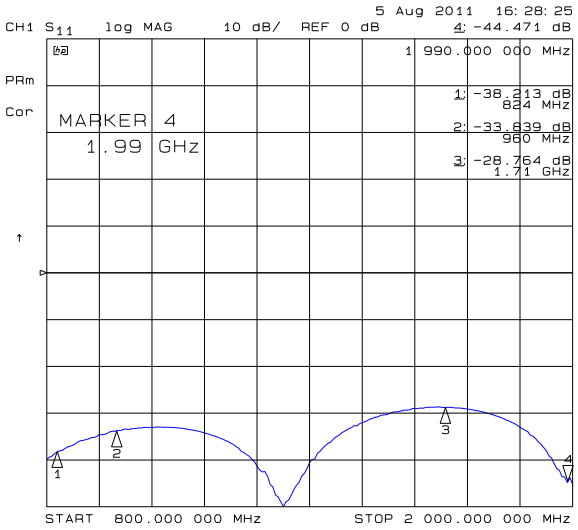
A characteristic impedance of nearly 50 Ω is achieved using trace width = 1.1 mm, clearance from coplanar ground plane = 0.3 mm each side. The line uses reference ground plane on layer 3, while copper is removed from layer 2 underneath the line. Height of trace above ground plane is 1.335 mm. Calculated characteristic impedance is 51.6 Ω, estimated line loss is less than 0.1 dB. The line geometry is shown below:



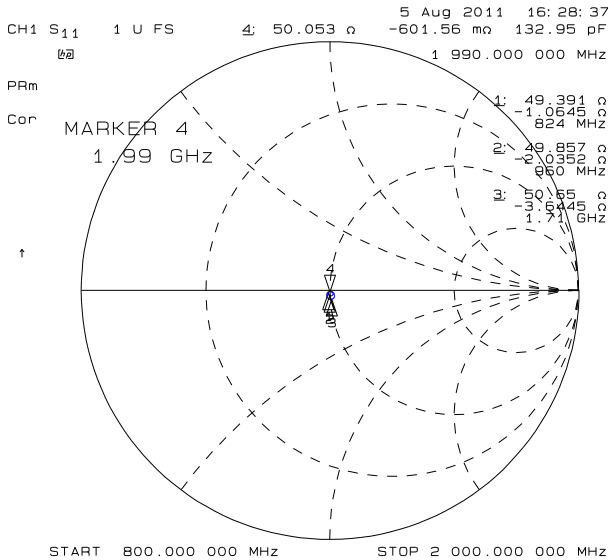
7.2.2. Transmission line measurements

HP8753E VNA (Full-2-port calibration) has been used in this measurement session. A calibrated coaxial cable has been soldered at the pad corresponding to GE866-QUAD RF output; a SMA connector has been soldered to the board in order to characterize the losses of the transmission line including the connector itself. During Return Loss / impedance measurements, the transmission line has been terminated to 50 Ω load.

Return Loss plot of line under test is shown below:



Line input impedance (in Smith Chart format, once the line has been terminated to 50 Ω load) is shown in the following figure:



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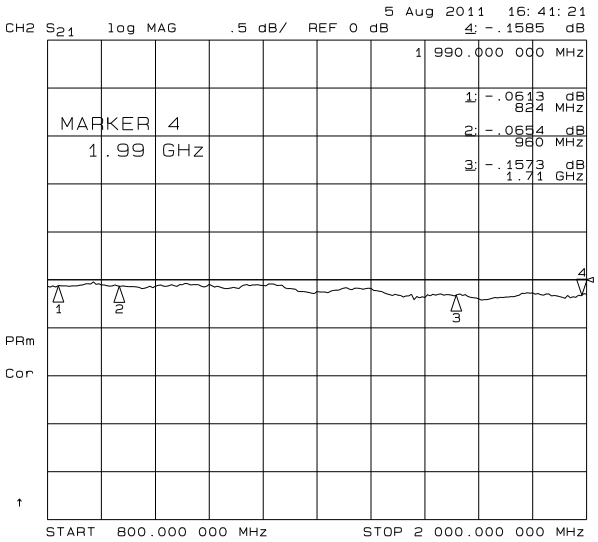
Insertion Loss of G-CPW line plus SMA connector is shown below:



7.3. GSM Antenna - installation Guidelines

- Install the antenna in a place covered by the GSM signal.
- Antenna shall not be installed inside metal cases
- Antenna shall be installed also according to antenna manufacturer instructions.
- Ddd Installation should also take in account the R&TTE requirements described in the "Conformity Assessment Issues" chapter

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8. Logic levels specifications

Where not specifically stated, all the interface circuits work at 1.8V CMOS logic levels. The following table shows the logic level specifications used in the GE866-QUAD interface circuits:

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) when on	-0.3V	+2.1V

Level	Min	Max
Input high level	1.3V	1.9V
Input low level	0V	0.35V
Output high level	1.6V	1.9V
Output low level	0V	0.2V

Level	Typical
Output Current	1mA
Input Current	1uA

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8.1. Reset signal

Signal	Function	I/O	pin
RESET*	Phone reset	I	G4

RESET* is used to reset the GE866-QUAD. Whenever this signal is pulled low, the GE866-QUAD is reset. When the device is reset it stops any operation. After the release of the reset GE866-QUAD is unconditionally shut down, without doing any detach operation from the network where it is registered. This behaviour is not a proper shut down because any GSM device is requested to issue a detach request on turn off. For this reason the Reset signal must not be used to normally shutting down the device, but only as an emergency exit in the rare case the device remains stuck waiting for some network response.

The RESET* is internally controlled on start-up to achieve a proper power-on reset sequence, so there's no need to control this pin on start-up. It may only be used to reset a device already on that is not responding to any command.

NOTE:

Do not use this signal to power OFF the GE866-QUAD. Use the ON/OFF procedure to perform this function.

Signal	Min	Max
RESET* Input high	1.8V(NOTE1)	2.1V
RESET* Input low	0V	0.2V

(NOTE1) this signal is internally pulled up so the pin can be left floating if not used.

If unused, this signal may be left unconnected. If used, then it must always be connected with an open collector transistor, to permit to the internal circuitry the power on reset and under voltage lockout functions.

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9. Serial Ports

The serial port on the GE866-QUAD is the core of the interface between the module and OEM hardware.

2 serial ports are available on the module:

- MODEM SERIAL PORT 1 (Main, ASC0)
- MODEM SERIAL PORT 2 (Auxiliary, ASC1)

9.1. Modem Serial Port

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- microcontroller UART @ 1.8V (Universal Asynchronous Receive Transmit)
- microcontroller UART @ 3V or other voltages different from 1.8V
- microcontroller UART @ 5V or other voltages different from 1.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work. The only configuration that doesn't need a level translation is the 1.8V UART.

The serial port on the GE866-QUAD is a +1.8V UART with all the 8 RS232 signals. It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels. The levels for the GE866-QUAD UART are the CMOS levels:

Parameter	Min	Max
Input level on any digital pad when on	-0.3V	+2.1V
Input voltage on analog pads when on	-0.3V	+2.1V

Level		Min	Max
Input high level	V_{IH}	1.5V	1.9V
Input low level	V_{IL}	0V	0.35V

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Output high level V_{OH}	1.6V	1.9V
Output low level V_{OL}	0V	0.2V

The signals of the GE866-QUAD serial port are:

RS232 Pin Number	Signal	GE866-QUAD Pad Number	Name	Usage
1	DCD - dcd_uart	B2	Data Carrier Detect	Output from the GE866-QUAD that indicates the carrier presence
2	RXD - tx_uart	A5	Transmit line *see Note	Output transmit line of GE866-QUAD UART
3	TXD - rx_uart	A4	Receive line *see Note	Input receive of the GE866-QUAD UART
4	DTR - dtr_uart	A2	Data Terminal Ready	Input to the GE866-QUAD that controls the DTE READY condition
5	GND	D1, F1, G1, D2, F2, C2, E3, F3, G3	Ground	Ground
6	DSR - dsr_uart	A3	Data Set Ready	Output from the GE866-QUAD that indicates the module is ready
7	RTS - rts_uart	A1	Request to Send	Input to the GE866-QUAD that controls the Hardware flow control
8	CTS - cts_uart	B1	Clear to Send	Output from the GE866-QUAD that controls the Hardware flow control
9	RI - ri_uart	B3	Ring Indicator	Output from the GE866-QUAD that indicates the incoming call condition

NOTE:

According to V.24, RX/TX signal names are referred to the application side, therefore on the GE866-QUAD side these signal are on the opposite direction: TXD on the application side will be connected to the receive line (here named TXD/ rx_uart) of the GE866-QUAD serial port and vice versa for RX.

NOTE:

For a minimum implementation, only the TXD and RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the GE866-QUAD when the module is powered off or during an ON/OFF transition.

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9.2. RS232 levels translation

In order to interface the GE866-QUAD with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must:

- invert the electrical signal in both directions;
- change the level from 0/1.8V to +15/-15V

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.

The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).

By convention the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART.

In order to translate the whole set of control lines of the UART you will need:

- 5 drivers
- 3 receivers

NOTE:

The digital input lines working at 1.8V CMOS have an absolute maximum input voltage of 2.1V; therefore the level translator IC shall not be powered by the +3.8V supply of the module. Instead, it must be powered from a +1.8V (dedicated) power supply.

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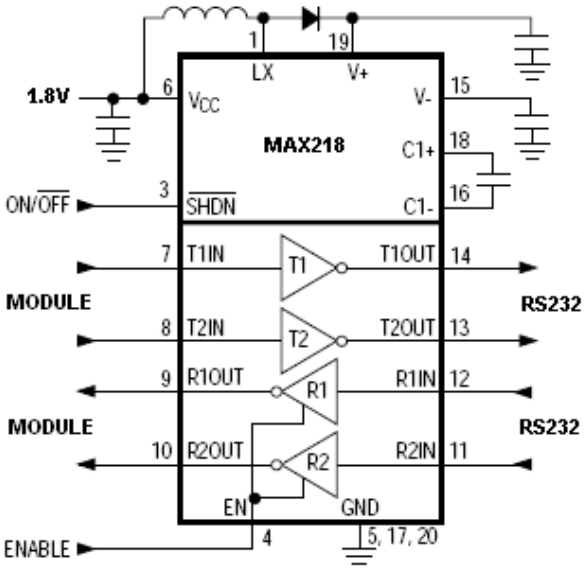
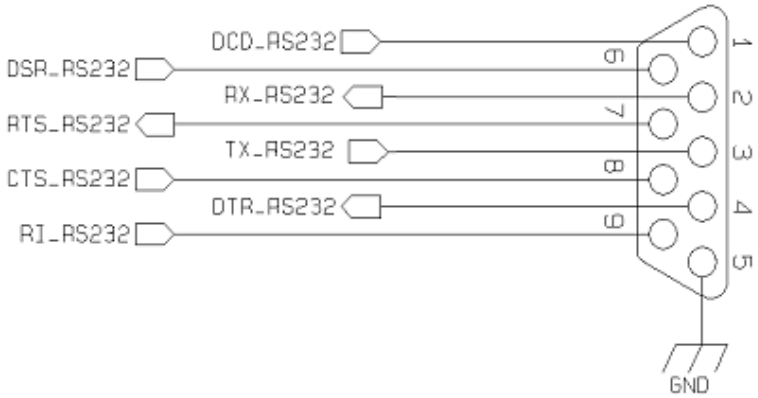
An example of RS232 level adaptation circuitry could be done using a MAXIM transceiver (MAX218).

In this case the chipset is capable to translate directly from 0/1.8V to the RS232 levels (Example done on 4 signals only).



The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



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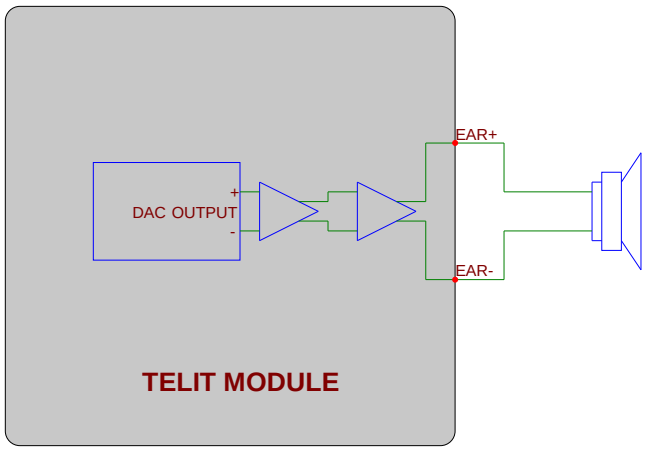
10. Audio Section Overview

10.1. MIC Connection

The Base Band Chip of the GE866-QUAD provides one input for audio to be transmitted (*Uplink*).

10.2. EAR Connection



The audio output of the GE866-QUAD is balanced, this is helpful to double the level and to reject common mode (click and pop are common mode and therefore rejected); furthermore the output stage is class-D, so it can manage directly a loudspeaker with electrical impedance of at least 8Ohm. This stage is powered by switching from Vbatt to gnd at a frequency ranging from 0.6 to 2MHz, so it has a good efficiency and thus a big power budget 0.7W; being a class-D architecture, please use some caution (see the NOTE below).

NOTE:

When the loudspeaker is connected with a long cable, an L-C filter is recommended.

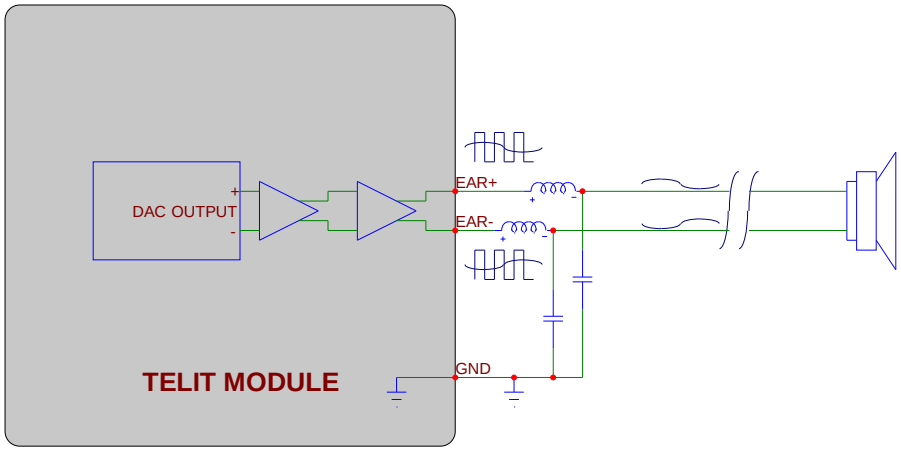
When the EAR+/- are feeding some electronic circuitry, an R-C filter is recommended.

TIP:

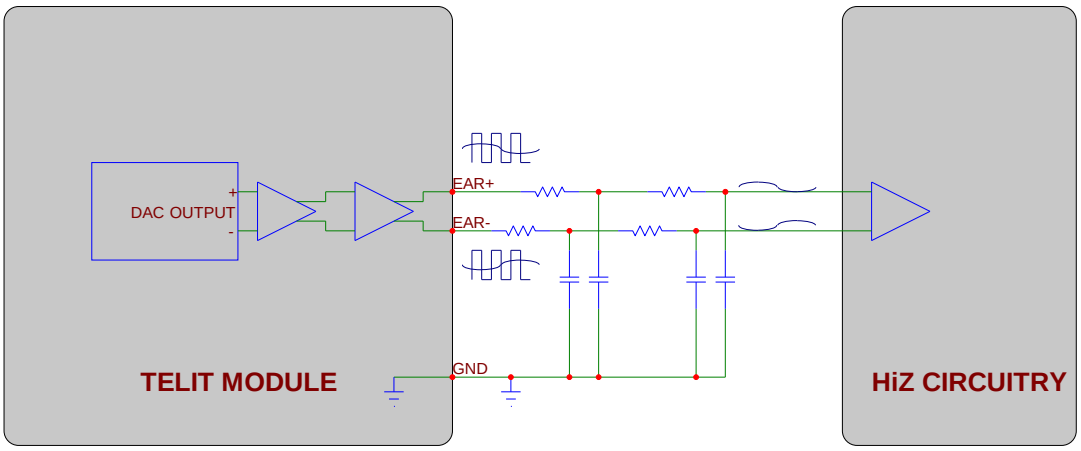
In order to get the maximum audio level at a given output voltage level (dBspl/Vrms), the following breaking through procedure can be used. Have the loudspeaker as close as you can to the listener (this simplify also the echo cancelling); choose the loudspeaker with the higher sensitivity (dBspl per W); choose loudspeakers with the impedance close to the limit (ex: 16 or 8 Ohm), in order to feed more power inside the transducer (it increases the W/Vrms ratio). If this were not enough, an external amplifier should be used.

WARNING:

This The audio output hardware of the GE866-QUAD is based on a Class-D amplifier so any singled-end output configuration MUST NOT BE USED, otherwise the presence of GSM buzzing and low level audio performance will result.



L-C filtering for LOW impedance load.



R-C filtering for HIGH impedance load.

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10.3. Electrical Characteristics

10.3.1. Input lines

Microphone/Line-in path	
Line Type	Differential
Coupling capacitor	≥ 100nF
Differential input resistance	50kΩ
Levels	
To have 0 dBfs @1KHz *(*)*	Differential input voltage
MIC Gain = 0dB	290mVrms
MIC Gain = +6dB	145mVrms
MIC Gain = +12dB	72mVrms
MIC Gain = +18dB	36mVrms
MIC Gain = +24dB	18mVrms
MIC Gain = +30dB	9mVrms
MIC Gain = +36dB	4.5mVrms
MIC Gain = +42dB	2.25mVrms

(*) 0 dBfs in the network are +3.14 dBm0

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10.3.2. Output lines

EAR/Line-out Output	
Differential line coupling	Direct connection (V_{DC}=1.7÷2.1V)
output load resistance	≥ 8 Ω
signal bandwidth	250÷3400Hz *(@ -3dB with default filter)*
max. differential output voltage	1120 mV_{pp} *@3.14dBm0 (*)*
differential output voltage	550mV_{rms} *@0dBm0 (*)*
volume increment	2dB per step
volume steps	0..10

(*) in default condition: Output Volume = +20dB, Output Attenuation = 0dB

TIP:

We suggest driving the load differentially; this kills all the common mode noises (click and pop, for example), the output swing will double (+6dB) and the big output coupling capacitor will be avoided.

In order to get the maximum power output from the device, the resistance of the tracks has to be negligible in comparison to the load.

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11. General Purpose I/O

The general purpose I/O pads can be configured to act in three different ways:

- input
- output
- alternate function (internally controlled)

Input pads can be read; they report the digital value (high or low) present on the pad at the read time.

Output pads can only be written or queried and set the value of the pad output.

An *alternate function* pad is internally controlled by the GE866-QUAD firmware and acts depending on the function implemented.

For Logic levels please refer to chapter 8.

The following table shows the available GPIO on the GE866-QUAD.

Pin	Signal	I/O	Function	Type	Input / output current	Default State	ON_OFF state	State during Reset	Note
C5	GPIO_01	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function DVI_WA0
C6	GPIO_02	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function JDR and DVI_RX
D6	GPIO_03	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function DVI_TX
D5	GPIO_04	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function TX Disable and DVI_TX
B5	GPIO_05	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function RFTXMON
B4	GPIO_06	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function ALARM / BUZZER
C4	GPIO_07	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function STAT_LED

WARNING:

During power up the GPIOs may be subject to transient glitches.

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Also the UART's control flow pins can be used as GPIO.

Pin	Signal	I/O	Function	Type	Input / output current	Default State	ON_OFF state	State during Reset	Note
B2	GPO_A	O	Configurable GPO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function C109/DCD
B3	GPO_B	O	Configurable GPO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function C125/RING
A3	GPO_C	O	Configurable GPO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function C107/DSR
A2	GPI_E	I	Configurable GPI	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function C108/DTR
A1	GPI_F	I	Configurable GPI	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function C105/RTS
B1	GPO_D	O	Configurable GPO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function C106/CTS

11.1. GPIO Logic Levels

Where not specifically stated, all the interface circuits work at 1.8V CMOS logic levels.

The following table shows the logic level specifications used in the GE866-QUAD interface circuits:

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) when on	-0.3V	+2.1V

Level	Min	Max
Input high level	1.5V	1.9V
Input low level	0V	0.35V
Output high level	1.6V	1.9V
Output low level	0V	0.2V

Level	Typical
Output Current	1mA
Input Current	1uA

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11.2. Using a GPIO Pad as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO.

If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 1.8V CMOS, then it can be buffered with an open collector transistor with a 47K pull up to 1.8V.

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the GE866-QUAD when the module is powered OFF or during an ON/OFF transition.

TIP:

The V_AUX / PWRMON pin can be used for input pull up reference or/and for ON monitoring.

11.3. Using a GPIO Pad as OUTPUT

The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

11.4. Using the RF Transmission Control GPIO4

The GPIO4 pin, when configured as RF Transmission Control Input, permits to disable the Transmitter when the GPIO is set to Low by the application.

In the design is necessary to add a resistor 47K pull up to 2.8V, this pull up must be switched off when the module is in off condition.

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11.5. Using the RFTXMON Output GPIO5

The GPIO5 pin, when configured as RFTXMON Output, is controlled by the GE866-QUAD module and will rise when the transmitter is active and fall after the transmitter activity is completed.

There are 2 different modes for this function:

1) **Active during the Call:**

For example, if a call is started, the line will be HIGH during all the conversation and it will be again LOW after hanged up.

The line rises up 300ms before first TX burst and will became again LOW from 500ms to 1s after last TX burst.

2) **Active during the TX activity**

The GPIO is following the TX bursts

Please refer to the AT User interface manual for additional information on how to enable this function.

11.6. Using the ALARM/BUZZER output GPIO6

The GPIO6 has 2 alternate functions:

- ALARM
- BUZZER

The GPIO6 pad, when configured as ***Alarm Output***, is controlled by the GE866-QUAD module and will rise when the alarm starts and fall after the issue of a dedicated AT command.

This output can be used to controlling microcontroller or application at the alarm time.

The GPIO6 pad, when configured as ***Buzzer Output***, is controlled by the GE866-QUAD module and will drive a Buzzer driver with appropriate square waves.

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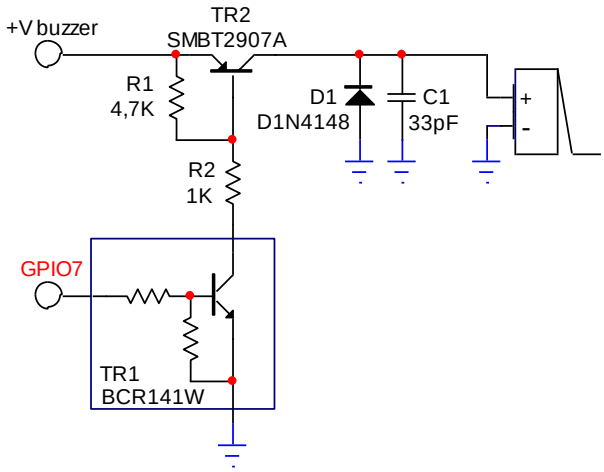
This permits to your application to easily implement Buzzer feature with ringing tones or melody played at the call incoming, tone playing on SMS incoming or simply playing a tone or melody when needed.

A sample interface scheme is included below to give you an idea of how to interface a Buzzer to the GPIO6:



NOTE:

To correctly drive a buzzer a driver must be provided, its characteristics depend on the Buzzer and for them refer to your buzzer vendor

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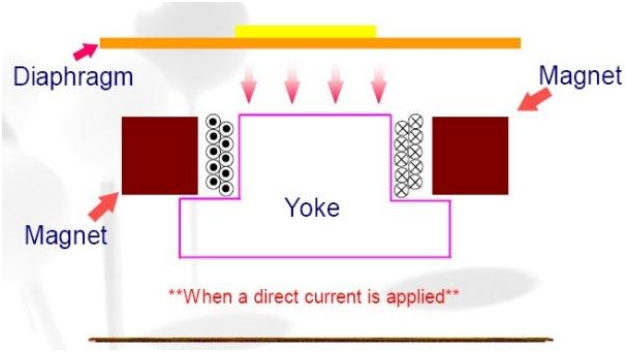
11.7. Magnetic Buzzer Concepts

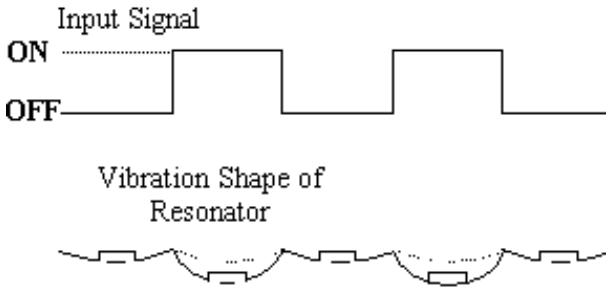
11.7.1. Short Description

A magnetic Buzzer is a sound-generating device with a coil located in the magnetic circuit consisting of a permanent magnet, an iron core, a high permeable metal disk and a vibrating diaphragm.



Drawing of the Magnetic Buzzer.

The disk and diaphragm are attracted to the core by the magnetic field. When an oscillating signal is moved through the coil, it produces a fluctuating magnetic field which vibrates the diaphragm at the frequency of the drive signal. Thus the sound is produced relative to the frequency applied.



Diaphragm movement.

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11.7.2. Frequency Behaviour

The frequency behavior represents the effectiveness of the reproduction of the applied signals. Because performance is related to a square driving waveform (whose amplitude varies from 0V to Vpp), if you modify the waveform (e.g. from square to sinus) the frequency response will change.

11.7.3. Power Supply Influence

Applying a signal whose amplitude is different from that suggested by the manufacturer, the performance change following the rule "if resonance frequency fo increases, amplitude decreases".

Because resonance frequency depends on acoustic design, by lowering the amplitude of the driving signal the response bandwidth tends to become narrow, and vice versa.

Summarizing: $V_{pp} \uparrow \rightarrow f_o \downarrow$ $V_{pp} \downarrow \rightarrow f_o \uparrow$

The risk is that the fo could easily fall outside of new bandwidth; consequently the SPL could be much lower than the expected.

WARNING:

It is very important to respect the sense of the applied voltage: never apply to the "-" pin a voltage more positive than the "+" pin: if this happens, the diaphragm vibrates in the opposite direction with a high probability to be expelled from its physical position. This damages the device permanently.

11.7.4. Working Current Influence

In the component data sheet you will find the value of MAX CURRENT: this represents the maximum average current that can flow at nominal voltage without current limitation. In other words it is not the peak current, which could be twice or three times higher. If driving circuitry does not support these peak values, the SPL will never reach the declared level or the oscillations will stop.

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11.8. STAT LED Indication of network service availability

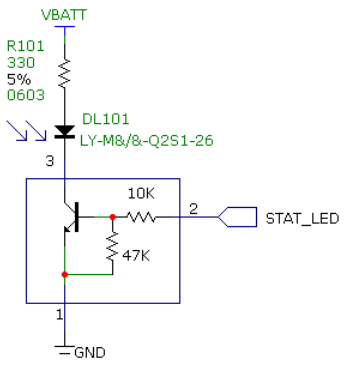
The STAT_LED pin status shows information on the network service availability and Call status.

In the GE866-QUAD modules, the STAT_LED usually needs an external transistor to drive an external LED.

Therefore, the status indicated in the following table is reversed with respect to the pin status.

LED status	Device Status
Permanently off	Device off
Fast blinking (Period 1s, Ton 0,5s)	Net search / Not registered / turning off
Slow blinking (Period 3s, Ton 0,3s)	Registered full service
Permanently on	a call is active

A schematic example could be:



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11.9. SIMIN detect function

All the GPIO pins can be used as SIM DETECT input. The AT Command used to enable the function is:

AT#SIMINCFG

Use the AT command **AT#SIMDET=2** to enable the SIMIN detection

Use the AT command **AT&W0** and **AT&P0** to store the SIMIN detection **in the common profile.**

For full details see AT Commands Reference Guide, 80000ST10025a.

NOTE:

Don't use the SIM IN function on the same pin where the GPIO function is enabled and vice versa!

11.10. RTC Bypass out

The VRTC pin brings out the Real Time Clock supply, which is separate from the rest of the digital part, allowing having only RTC going on when all the other parts of the device are off.

To this power output a backup battery can be added in order to increase the RTC autonomy during power off of the main battery (power supply). NO Devices must be powered from this pin.

11.11. SIM Holder Implementation

Please refer to the related User Guide (SIM Holder Design Guides, 80000NT10001a).

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12. DAC and ADC section

12.1. DAC Converter

12.1.1. Description

The GE866-QUAD provides a Digital to Analog Converter. The signal (named DAC_OUT) is available on pin E4 of the GE866-QUAD.

The on board DAC is a 10 bit converter, able to generate an analogue value based on a specific input in the range from 0 up to 1023. However, an external low-pass filter is necessary

	Min	Max	Units
Voltage range (filtered)	0	1.8	Volt
Range	0	1023	Steps

The precision is 10 bits so, if we consider that the maximum voltage is 2V, the integrated voltage could be calculated with the following formula:

Integrated output voltage = (2 *value) / 1023

DAC_OUT line must be integrated (for example with a low band pass filter) in order to obtain an analog voltage.

12.1.2. Enabling DAC

An AT command is available to use the DAC function.

The command is: **AT#DAC= [**<enable> **[**, <value>**]]**

<**value**> - scale factor of the integrated output voltage (0..1023 - 10 bit precision)

it must be present if <**enable**>=**1**

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

NOTE:

The DAC frequency is selected internally. D/A converter must not be used during POWERSAVING.

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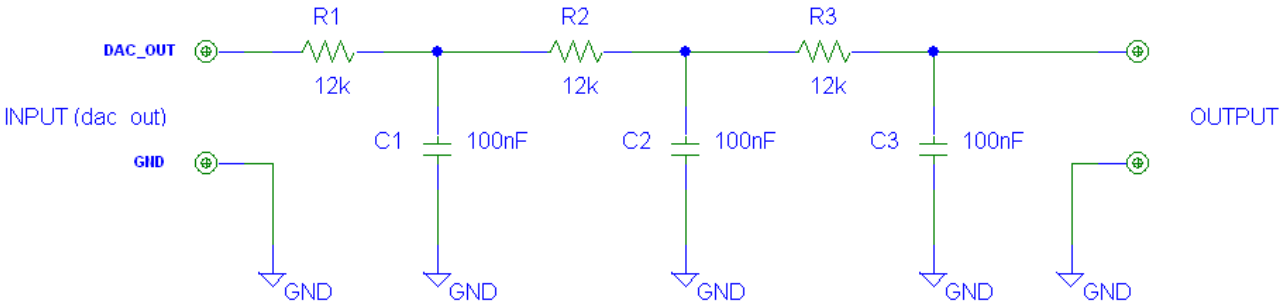
12.1.3. Low Pass Filter Example



12.2. ADC Converter

12.2.1. Description

The on board A/D converter is a 11-bit converter. It's able to read a voltage level in the range of 0÷2 volts applied on the ADC pin input, store and convert it into 11 bit word.

	Min	Max	Units
Input Voltage range	0	1.2	Volt
AD conversion	-	10	bits
Resolution	-	> 1	mV

The GE866-QUAD module provides one Analog to Digital Converters.

The input line is:

ADC_IN

Available on pin F4

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12.2.2. Using ADC Converter

An AT command is available to use the ADC function.

The command is **AT#ADC=1,2**

The read value is expressed in mV

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

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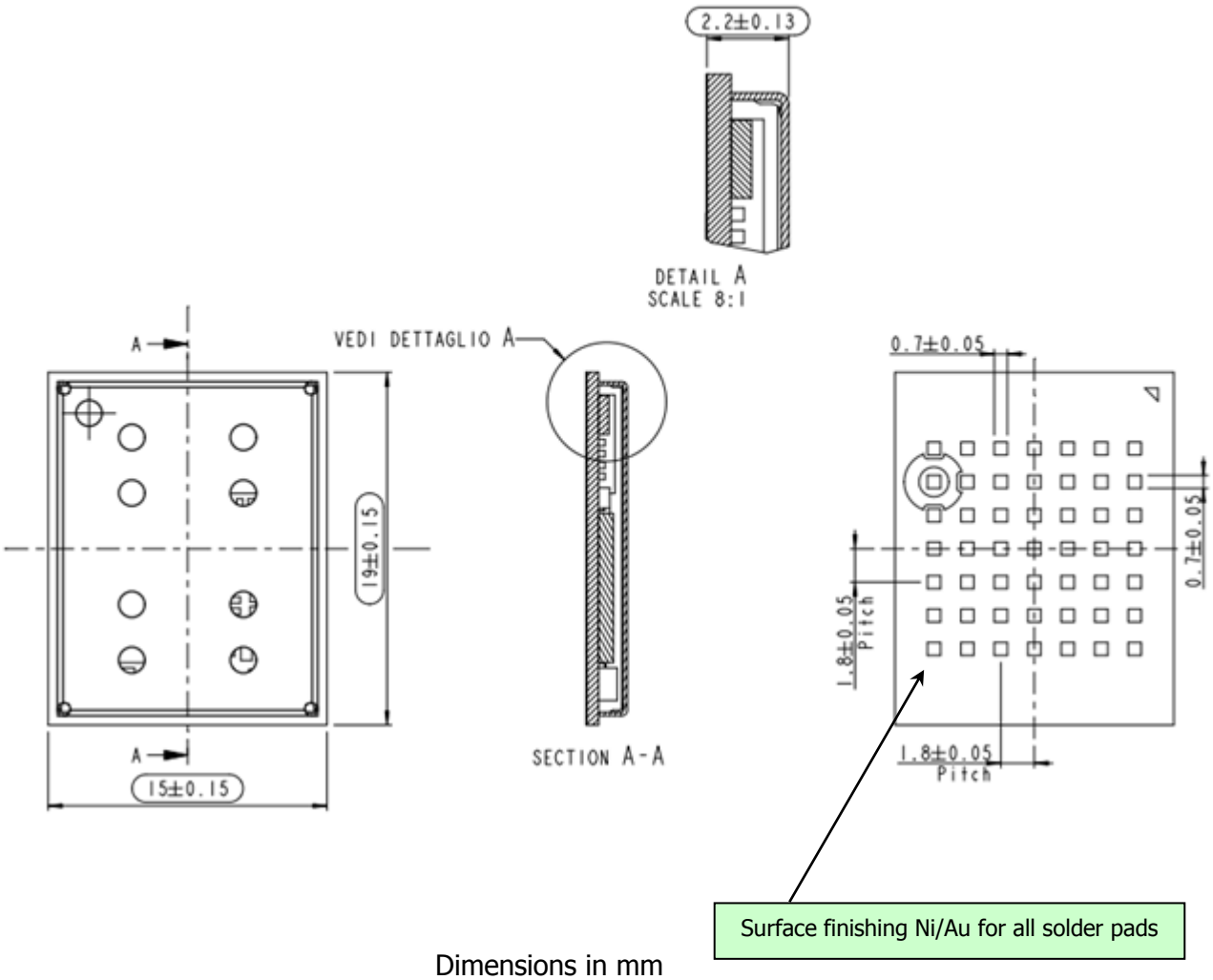
13. Mounting the GE866 on your Board

13.1. General

The GE866 modules have been designed in order to be compliant with a standard lead-free SMT process.

13.2. Module finishing & dimensions



Dimensions in mm

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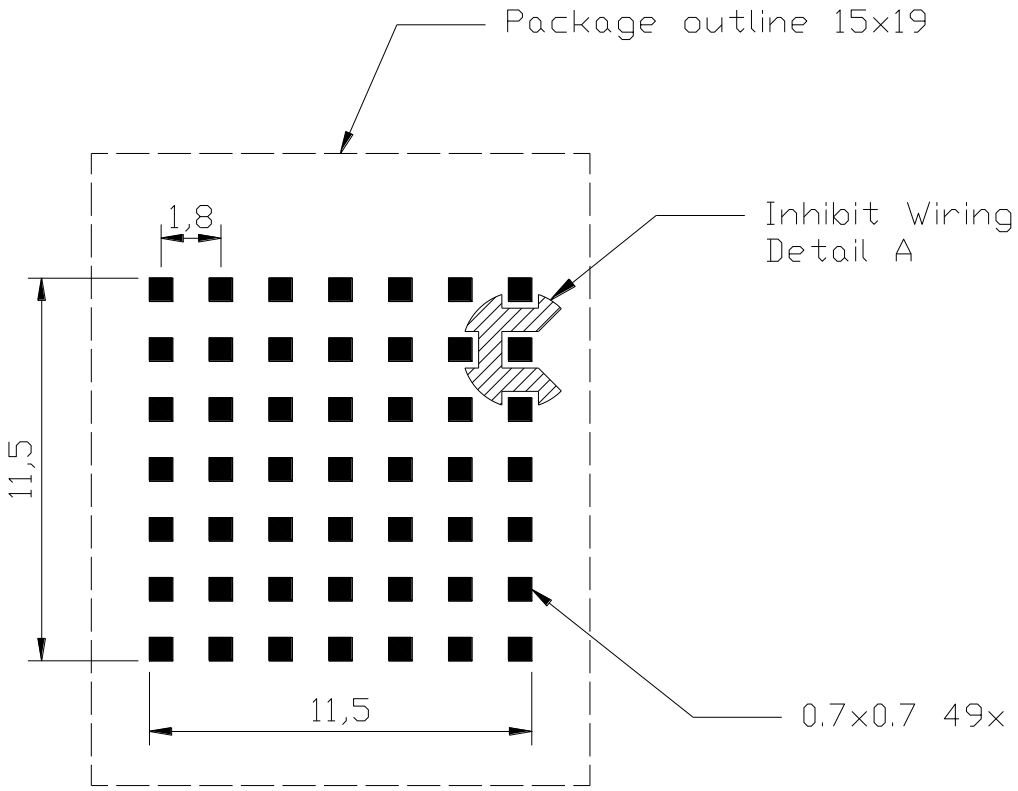
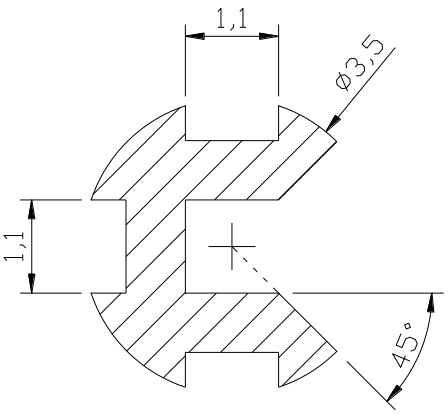
13.3. Recommended foot print for the application (dimensions in mm):



Copper pad pattern
Top view



Detail A

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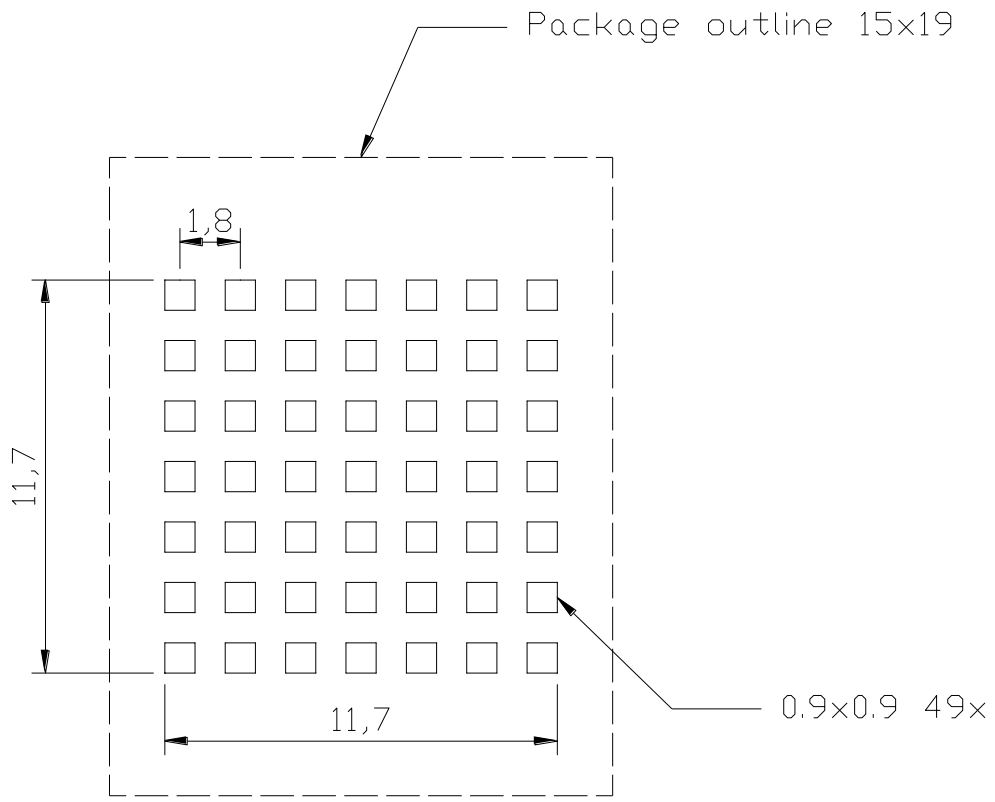

Solder resist pattern
Top view

In order to easily rework the GE866 is suggested to consider on the application a 1.5 mm placement inhibit area around the module.

It is also suggested, as common rule for an SMT component, to avoid having a mechanical parts of the application in direct contact with the module.

NOTE:

In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.

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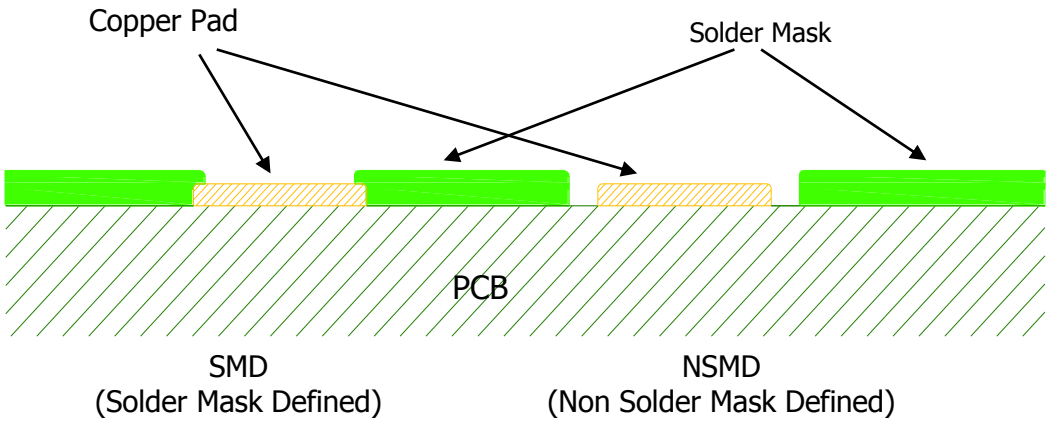
13.4. Stencil

Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil ≥ 120 µm.

13.5. PCB pad design

Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.



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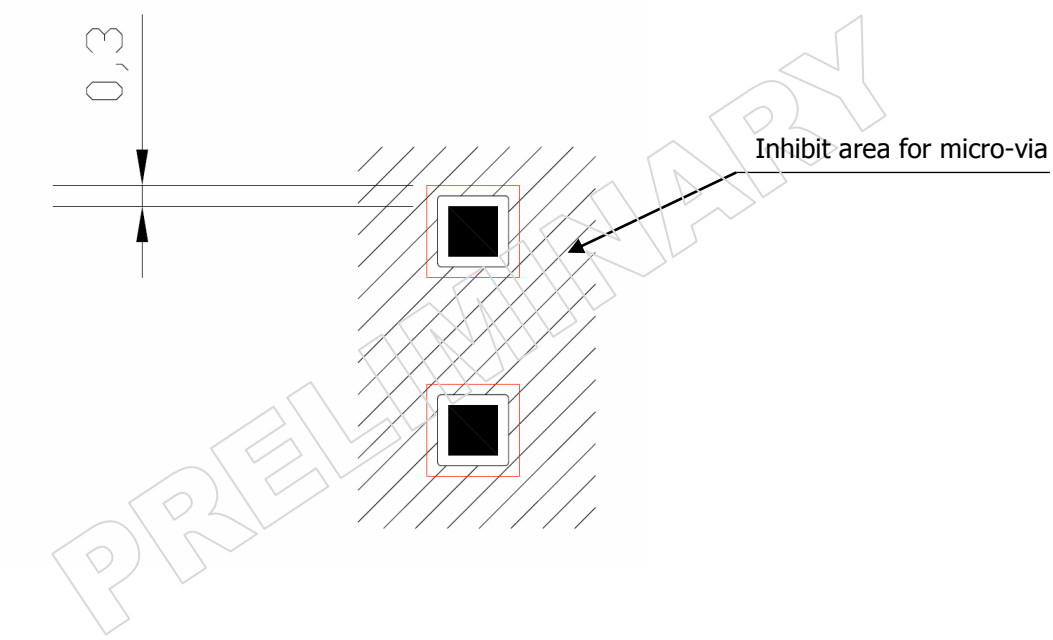
13.6. Recommendations for PCB pad dimensions (mm):

It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal of the pad itself (see following figure).



PRELIMINARY

Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

Finish	Layer thickness [µm]	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.03 – 0.15	Good solderability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

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It is not necessary to panel the application PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

13.7. Solder paste

	Lead free
Solder paste	Sn/Ag/Cu

We recommend using only "no clean" solder paste in order to avoid the cleaning of the modules after assembly.

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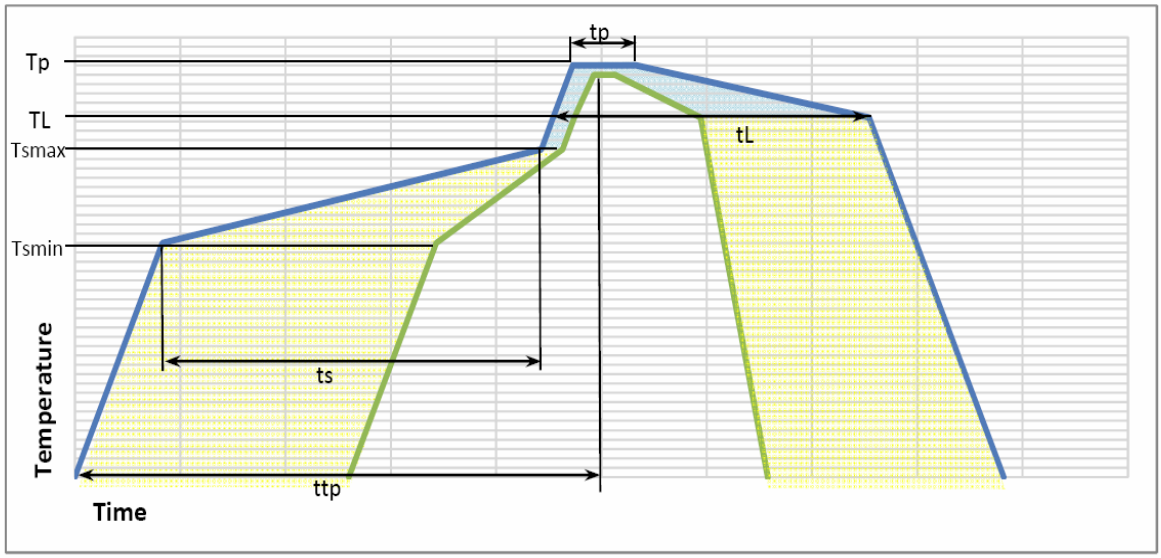
13.8. GE866 Solder reflow

Recommended solder reflow profile



Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to TP)	3°C/second max
Preheat – Temperature Min (Tsmin) – Temperature Max (Tsmax) – Time (min to max) (ts)	 150°C 200°C 60-180 seconds
Tsmax to TL – Ramp-up Rate	 3°C/second max
Time maintained above: – Temperature (TL) – Time (tL)	 217°C 60-150 seconds
Peak Temperature (Tp)	245 +0/-5°C
Time within 5°C of actual Peak	10-30 seconds

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Temperature (tp)	
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

NOTE:

All temperatures refer to topside of the package, measured on the package body surface

WARNING:

The GE866 module withstands one reflow process only.

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14. Packing system

14.1. Packing on reel

The GE866 modules are packaged on reels of ***500*** pieces each (TBC).

14.2. Packing on tray

The GE866 modules are packaged on trays of 50 pieces each when small quantities are required (i.e. for test and evaluation purposes). Trays are not designed to be used in SMT processes for pick and place handling.

WARNING:

These trays can withstand at the maximum temperature of 65° C.

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14.3. Moisture sensibility

The moisture sensitivity level of the Product is "3" according with standard IPC/JEDEC J-STD-020, take care of all the relative requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:

a) The shelf life of the Product inside of the dry bag is 12 months from the bag seal date, when stored in a non-condensing atmospheric environment of < 40°C and < 90% RH.
b) Environmental condition during the production: <= 30°C / 60% RH according to IPC/JEDEC J-STD-033B.
c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) "IPC/JEDEC J-STD-033B paragraph 5.2" is respected.
d) Baking is required if conditions b) or c) are not respected
e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

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15. Safety Recommendations

READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.
The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has
to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the electronic equipments introduced on the market. All the relevant information's are available on the European Community website:

http://ec.europa.eu/enterprise/sectors/rtte/documents/

The text of the Directive 99/05 regarding telecommunication equipments is available, while the applicable Directives (Low Voltage and EMC) are available at:

http://ec.europa.eu/enterprise/sectors/electrical/

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16. Document History

Revision	Date	Changes
Rev. 0	2013-10-02	First issue
Rev. 1	2014-02-07	Updated VRTC voltage, power consumption and packing system
Rev.2	2014-09-05	Updated Mechanical Dimensions
Rev.3	2014-09-10	Updated section 13 “Mounting the GE866 on your Board”

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